Amendments to the Drawings:

The attached new sheet of drawings includes new Fig. 1F.

New Figure 1F, shows a semiconductor device that includes: 1) a rear surface of a bridge that is recessed relative to the rear surface of the insulating resin; and 2) the rear surface of the bridge being covered by an insulating film.

Attachments following last page of this Amendment:

New Sheet (1 pages)

REMARKS

Drawing Objections:

The Examiner objected to the drawings for not showing in combination: 1) a rear surface of a bridge that is recessed relative to the rear surface of the insulating resin; and 2) the rear surface of the bridge being covered by an insulating film, as is recited in claim 4.

Applicants submit the attached new figure 1F, which shows a semiconductor device that includes, in combination: 1) a rear surface of a bridge 53 that is recessed relative to the rear surface of the insulating resin 61; and 2) the rear surface of the bridge 53 being covered by an insulating film 62.

Support for new figure 1F can be found, for example, on page 8, lines 17-18, which states, "like the case of FIG. 1C, the rear surface of the semiconductor device [of FIG. 1D] is covered with the insulating resin 62 so that only the areas of the O marks 92 may be exposed." No new matter is being added.

Applicants respectfully request acceptance of new figure 1F.

Failure to Comply with Written Description Requirement:

Claims 4, 23 and 28 were rejected for failing to comply with the written description requirement because the specification allegedly failed to disclose "wherein the rear surface of at least one bridge is recessed relative to the rear surface of the insulating resin," as recited in claim 4.

Applicants disagree and respectfully submit that examples of that feature are disclosed in both figure 1D and new figure 1F. In figure 1D, a rear surface of bridge 53 is recessed relative to a rear surface of the insulating resin (at 64). Similarly, in new figure 1F, a rear surface of bridge 53 is recessed relative to a rear surface of the insulating resin (at 64).

Applicants respectfully request withdrawal of the rejections for failure to comply with the written description requirement.

Claim Rejections – Prior Art:

Claims 4 and 28 were rejected as being unpatentable over the combination of U.S. Patent No. 5,273,938 (Lin et al.) and U.S. Patent No. 5,352,632 (Sawaya).

Claim 4 has been amended to recite that an entire rear surface of the semiconductor device is covered by an insulating film except for a part of the rear surface that is an external connecting electrode. Support for that amendment can be found, for example, in FIG. 2A and FIG. 2C and on page 8, line 26-page 9, line 9. No new matter has been added. Certain implementations of the features now recited in claim 4 may result in a semiconductor device, in which the likelihood of short circuits occurring is reduced. Neither the Lin et al. patent nor the Sawaya patent disclose or suggest that feature.

The Lin et al. patent discloses a semiconductor device that includes a two semiconductor die 15, 17. (*See* FIG. 3) Each semiconductor die 15, 17 is attached to a respective die receiving portion 19. A conductive trace 13 is positioned between the semiconductor die 15, 17 and electrically connects them to each other. Conductive traces 13 also are positioned outside the semiconductor die 15, 17. FIG. 6 shows that an exposed surface of those conductive traces 13 can be attached to solder balls 26. Wire bonds 18 electrically connect each die 15, 17 to one of the conductive traces 13 positioned outside the semiconductor die 15, 17. (*See* FIG. 3) Wire bonds 18 also electrically connect the two semiconductor die 15, 17 to the conductive trace 13 that is located between the semiconductor die 15, 17. Insulating resin 20 seals both semiconductor die 15, 17, the conductive trace 13 that is located between the semiconductor die 15, 17 and the wire bonds 18. The insulating resin 20 separates the die receiving portions 19 from adjacent conductive traces 13. Recesses are formed in a rear surface of the insulating resin. (*See* FIG. 3) The die receiving portions 19 and the conductive traces 13 are exposed through those recesses.

The Lin et al. patent does not disclose an insulating film that covers an entire rear surface of the semiconductor die 15, 17 except for a part of the rear surface for external connecting electrodes. First, the insulating resin 20 is not a film. Additionally, the insulating resin 20 does not cover an entire rear surface of the semiconductor die 15, 17 except for a part of the rear surface that is an external connecting electrode.

The Sawaya patent discloses a semiconductor device (*see* FIG. 13) that includes a second lead section 13B with an upper surface that is recessed relative to the upper surface of the

package 15, which is resin. The upper surface of the second lead section 13B is covered with a resin tape 14. The Sawaya et al. patent does not disclose an insulating film that covers an entire rear surface of the semiconductor device except for a part of the rear surface for external connecting electrodes.

Claim 4 should be allowable for at least the foregoing reasons.

Claim 28 depends from claim 4 and, therefore, should be allowable for at least the same reasons as claim 4.

Claim 23 was rejected as being unpatentable over the Lin et al. patent and the Sawaya patent as applied to claim 4 above and further in view of U.S. Patent No. 6,001,671 (Fjelstad).

Claim 23 depends from claim 4, which recites that an entire rear surface of the semiconductor device is covered by an insulating film except for a part of the rear surface of the external connecting electrodes. As discussed above neither the Lin et al. patent nor the Sawaya patent disclose or suggest that feature. Nor does the Fjelstad et al. patent disclose or suggest that feature.

FIG. 2E of the Fjelstad et al. patent discloses a semiconductor package that includes semiconductor chip 120'. (*See* FIG. 2A-2E) A back surface 122' of a semiconductor chip 120' is bonded to a conductive region 115' through the use of the thermally conductive die attach adhesive 135'. The chip contacts (not shown) on the exposed face surface 121' of the chip 120' are then electrically connected to respective pads 110' by wirebonding wires 130' therebetween portions of a polymer sheet 100' that protrude from a rear surface of encapsulant 140' to form recesses at central conductive region 115' and pads 110'. (*See* FIG. 2A-2E) The central conductive region 115' is typically connected to a printed circuit board in such a way that heat is drawn away from the chip 120' during operation.

The polymer sheet 100' (see FIG. 2E) does not cover an entire rear surface of the chip 120' except for a part of the rear surface of the external connecting electrodes 110'. The polymer sheet 100' also does not cover part of the central thermally conductive region 115'.

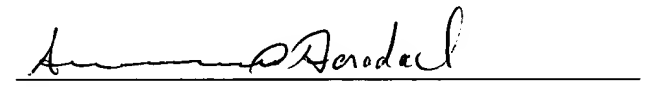
Claim 23 should be allowable for at least the foregoing reasons.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a $120 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: December 8, 2005



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